AMENDMENTS TO THE CLAIMS

Claims 1-2 (Cancelled)

3. (Previously Presented) A semiconductor circuit comprising:

a first transistor having:

a first semiconductor region;

spaced-apart source and drain regions formed in the first semiconductor region;

a first channel defined between the source and drain regions, the first channel having a first channel length and a first dopant concentration;

a layer of first gate oxide formed over the first channel, the layer of first gate oxide having a thickness; and

a gate formed over the layer of first gate oxide;

the first transistor conducting more than a leakage current when the gate, the source, and the first semiconductor region are connected to a same potential;

a second transistor having:

a second semiconductor region;

spaced-apart source and drain regions formed in the second semiconductor region;

a second channel defined between the source and drain regions formed in the second semiconductor region, the second channel having a second channel length and a second dopant concentration;

a layer of second gate oxide formed over the second channel, the layer of second gate oxide having a thickness, the thickness of the layer of first gate oxide being substantially less than the thickness of the layer of second gate oxide; and

a gate formed over the layer of second gate oxide;

the second transistor being substantially non-conductive when the gate of the second transistor, the source of the second transistor, and the second semiconductor region are connected to a same potential, the first channel length being approximately 30 percent to 80 percent as long as the second channel length; and

a third transistor formed in the semiconductor material, the third transistor having a third channel and a layer of third gate oxide formed over the third channel, the third channel having a third channel length and a third dopant concentration, the layer of third gate oxide having a thickness, the third transistor being substantially non-conductive when zero volts are applied to the gate, the thickness of the layer of third gate oxide being substantially equal to the thickness of the layer of first gate oxide.

4. (Original) The circuit of claim 3 wherein the first dopant concentration is substantially equal to a sum of the second dopant concentration and a dopant concentration implanted into the third channel.

5. (Original) The circuit of claim 4 wherein the second and third transistors have source and drain regions of the same conductivity type, and the first transistor has source and drain regions of an opposite conductivity type.

6. (Original) The circuit of claim 4 wherein the first and third transistors have source and drain regions of the same conductivity type, and the second transistor has source and drain regions of an opposite conductivity type.

7. (Previously Presented) The circuit of claim 3 wherein the source and drain regions of the second transistor are spaced apart from the source and drain regions of the first transistor.

8. (Previously Presented) The circuit of claim 3 wherein the gate formed over the layer of second gate oxide does not contact the source or drain region of the second transistor.

9. (Currently Amended) The circuit of claim ~~3~~ 10 wherein the first channel length is approximately 30 percent to 80 percent as long as the second channel length.

10. (New) A semiconductor circuit comprising:

a first transistor having:

a first semiconductor region;

spaced-apart first source and drain regions formed in the first semiconductor region;

a first channel located between the first source and drain regions, the first channel having a first channel length;

a layer of first gate oxide formed over the first channel; and

a gate formed over the layer of first gate oxide to contact the layer of first gate oxide, the gate being spaced apart from the first source and drain regions;

the first transistor conducting more than a leakage current when the gate, the first source, and the first semiconductor region are connected to a same potential;

a second transistor having:

a second semiconductor region, the second semiconductor region having a first conductivity type and a dopant concentration;

spaced-apart second source and drain regions of a second conductivity type formed in the second semiconductor region;

a second channel located between the second source and drain regions, the second channel having a second channel length, the first conductivity

type, and a dopant concentration, no region of the first conductivity type with a dopant concentration substantially greater than the dopant concentration of the second semiconductor region lying between the second source and drain regions;

a layer of second gate oxide formed over the second channel; and

a gate formed over the layer of second gate oxide, the gate of the second transistor contacting the layer of second gate oxide;

the second transistor being substantially non-conductive when the gate of the second transistor, the second source, and the second semiconductor region are connected to a same potential, the first channel length being shorter than the second channel length.

11. (New) The semiconductor circuit of claim 10 wherein the layer of first gate oxide has a first thickness, and the layer of second gate oxide has a second thickness that is substantially greater than the layer of first gate oxide.

12. (New) The circuit of claim 10 and further comprising a third transistor, the third transistor having:

a third semiconductor region;

spaced-apart third source and drain regions formed in the third semiconductor region;

a third channel located between the third source and drain regions, the third channel having a dopant concentration;

a layer of third gate oxide formed over the third channel; and

a gate formed over the layer of third gate oxide, the gate of the third transistor contacting the layer of third gate oxide;

the third transistor being substantially non-conductive when the gate of the third transistor, the third source, and the third semiconductor region are connected to a same potential.

13. (New) The circuit of claim 12 wherein the first channel has a dopant concentration substantially equal to a sum of the dopant concentration of the second channel and the dopant concentration of the third channel.

14. (New) The circuit of claim 12 wherein the dopant concentration of the first transistor, the dopant concentration of the second transistor, and the dopant concentration of the third transistor are different.